What Is claimed is:

1. A method of manufacturing a layer sequence having a first and a second laterally confined structure, comprising the steps of:

providing a first layer on a first surface portion of a substrate, which first layer is doped with dopant of a first type of conductivity;

providing a second layer on a second surface portion of the substrate, which second layer is free of dopant of the first type of conductivity;

forming a third layer on the first layer, which third layer is free of dopant of the first type of conductivity;

forming a fourth layer on the second layer, which forth layer is doped with dopant of the first type of conductivity;

etching the first layer and the third layer, thereby patterning the first and third layer to form the first laterally confined structure; and

etching the second layer and the forth layer, thereby patterning the second and fourth layer to form the second laterally confined structure.

2. The method of manufacturing a layer sequence according to claim 1, wherein the second layer and the third layer are doped with dopant of a second type of conductivity differing from the first type of conductivity.

3. The method of manufacturing a layer sequence according to claim 2, wherein one of the first and second types of conductivity is n-type conductivity and the other one of the first and second types of conductivity is p-type conductivity.

4. The method of manufacturing a layer sequence according to any of claims 1, wherein patterning is carried out such that the width of the first laterally confined structure generally equals the width of the second laterally confined structure.

5. The method of manufacturing a layer sequence according to claim 4, wherein the patterning includes the etching and a lithography process.

6. The method of manufacturing a layer sequence according to claim 5, wherein the etching is carried out using an etching gas.

7. The method of manufacturing a layer sequence according to claim 6, wherein the etching is a plasma etching.

8. The method of manufacturing a layer sequence according to claim 1, wherein a silicon substrate is provided as the substrate.

9. The method of manufacturing a layer sequence according to claim 1, wherein an intermediate layer is formed between the first layer and the third layer, the intermediate layer serving as an etch stop layer when etching the third layer and serving as a mask when etching the first layer.

10. The method of manufacturing a layer sequence according to claim 1, the intermediate layer is formed between the second layer and the forth layer, the intermediate layer serving as an etch stop layer when etching the forth layer and serving as a mask when etching the second layer.

11. A method of manufacturing a layer sequence having a first and a second laterally confined structure, comprising the steps of:

providing a gate oxide layer on a substrate;

providing a polysilicon layer having an undoped portion to form a gate of a p-MOS transistor and a doped portion to form a gate of an n-MOS transistor;

providing a doped polysilicon layer over said undoped portion of said polysilicon layer; and

providing an undoped polysilicon layer over said undoped portion of said polysilicon layer.

12. The method of claim 11 further comprising a step of providing a hard mask layer over said polysilicon layer.

13. The method of claim 11 further comprising a step of providing a bottom antireflective coating over said doped polysilicon layer and said undoped polysilicon layer.

14. The method of claim 11 wherein said step of providing a doped polysilicon layer over said undoped portion of said polysilicon layer comprises doping said polysilicon layer over said undoped portion with approximately equal doping to said doped portion of said polysilicon layer.

15. The method of claim 11 further comprising a step of etching said gate of said p-MOS transistor and said gate of said n-MOS transistor to have approximately equal dimensions.

16. An integrated circuit having a p-MOS transistor and an n-MOS transistor, said integrated circuit comprising:

a gate oxide layer on a substrate;

polysilicon layer having an undoped portion to form a gate of a p-MOS transistor and a doped portion to form a gate of an n-MOS transistor;

a doped polysilicon layer over said undoped portion of said polysilicon layer; and

an undoped polysilicon layer over said undoped portion of said polysilicon layer.

17. The integrated circuit of claim 16 further comprising a hard mask layer provided over said polysilicon layer.

18. The integrated circuit of claim 16 further comprising a a bottom antireflective coating over said doped polysilicon layer and said undoped polysilicon layer.

19. The integrated circuit of claim 16 wherein said doped polysilicon layer over said undoped portion of said polysilicon layer comprises a doped polysilicon layer with approximately equal doping to said doped portion of said polysilicon layer.

20. The integrated circuit of claim 16 further comprising a gate of said p-MOS transistor and a gate of said n-MOS transistor having approximately equal dimensions after etching.